MANUFACTURING MICROSYSTEMS-ON-A-CHIP WITH A 5-LEVEL SURFACE MICROMACHINING TECHNOLOGY

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ABSTRACT

An agile microsystem manufacturing technology has been developed that provides unprecedented 5 levels of independent polysilicon surface-micromachine films for the designer [1]. Typical surface-micromachining processes offer a maximum of 3 levels, making this the most complex surface-micromachining process technology developed to date. Leveraged from the extensive infrastructure present in the microelectronics industry, the manufacturing method of polysilicon surface-micromachining offers similar advantages of high-volume, high-reliability, and batch-fabrication to microelectromechanical systems (MEMS) as has been accomplished with integrated circuits (ICs). These systems, comprised of microscopic-sized mechanical elements, are laying the foundation for a rapidly expanding, multi-billion dollar industry [2] which impacts the automotive, consumer product, and medical industries to name only a few.

KEYWORDS

Microelectromechanical Systems (MEMS); Polysilicon Micromachining; Surface Micromachining; Chemical-Mechanical Polishing (CMP)

1. Introduction

Polysilicon surface micromachining is a technology for manufacturing MicroElectroMechanical Systems (MEMS) which has, as its basis, the manufacturing methods and tool sets used to manufacture the integrated electronic circuit. Polysilicon surface-micromachining is one technology that can greatly benefit by increasing the number of layers currently available for design. The complexity of the devices that can be fabricated in a polysilicon surface-micromachining technology scales super-linearly with the number of layers, analogous to design with multiple integrated circuit (IC) metalization layers. Here, we present a methodology that extends Sandia's currently available 4-level SUMMiT [3] process to 5-levels, overcoming the limits of too few design layers. Examples of batch-fabricated devices fabricated by the 4-level process can be found elsewhere [4]. This 5-level process allows the design of extremely complex micromechanical functions, with concomitant increase in device reliability and robustness [5].

The technology utilizes some of the latest processes available to the IC world such as chemical mechanical polishing (CMP) for planarization. CMP has provided the means to overcome surface topography, historically the primary impediment to extension to additional levels. CMP has also been shown to greatly enhance the manufacturability of a surface-micromachining technology in the precursory 4-level technology and is considered indispensable to the 5-level technology. In addition, film optimization for mechanical properties allows the fabrication of structures with

millimeter span and micrometer dimension features. The addition of independent layers available to the designer not only impacts the overall complexity of the devices, but also impacts the function, reliability, and robustness. For example, an accelerometer with spring and proof mass can be realized in a single level. However, the additional levels provide signal transduction, protective stops for mechanical over-stress, and force rebalance mechanisms. In another example, complex machinery consisting of actuators with rotating elements on movable platforms can be realized only if sufficient independent design levels are present. This highly manufacturable technology has already been used to realize MEMS and has potential as an agile manufacturing method for new MEMS designs.

2. Fabrication Technology and Facilities

Polysilicon surface micromachining uses the planar fabrication techniques common to the microelectronic circuit fabrication industry to manufacture micromechanical devices. The standard building-block process consists of depositing and photolithographically patterning alternate layers of low-stress polycrystalline silicon and sacrificial silicon dioxide. Vias etched through the sacrificial layers provide anchor points between the mechanical layers and the substrate. At the completion of the process, the sacrificial layers are selectively etched away in hydrofluoric acid (HF), which does not attack the polysilicon layers.

The result is a construction system consisting of one layer of polysilicon which provides electrical interconnection and one or more independent layers of mechanical polysilicon which can be used to form mechanical elements ranging from simple cantilevered beams to complex systems of springs, linkages, mass elements and joints. Typical in-plane lateral dimensions can be from one micron to several hundred microns, while the film thicknesses are typically in the range of two to four microns. Because the entire process is based on standard integrated-circuit fabrication technology, hundreds to thousands of devices can be batch-fabricated, fully assembled (without the need for piece-part assembly) on a single six-inch silicon substrate.

The continued inclusion of advanced IC process techniques in the manufacturing process for micromechanical devices was essential to the 5-level process development. For example, consistent yield and high-reliability with 3 (or greater)-level polysilicon surface-micromachining requires planarization of surface topography. This topography, which arises from the repetitive cycle of deposition and selective removal of films used to construct the micromachines, severely curtails advancement beyond a 3-layer process. In fact, 5-layers would be virtually impossible without planarization. Chemical-mechanical polishing (CMP) which is widely used in multi-level metalization for high-density, sub-micron integrated circuits has been extremely successful for planarization in polysilicon surface-micromachining [6].

3. Process Development

The 5-level technology has, as its basic process module, the repetitive cycle of deposition and definition of two primary films: a sacrificial silicon dioxide film and a structural polycrystalline silicon film. The deposition, photolithography, and etch processes are based on those used in standard IC fabrication, but modified for thicker, mechanically-optimized films. The common IC processes of low-pressure chemical vapor deposition (LPCVD) of polysilicon and silicon dioxide films, and reactive ion etch for film definition are used. A 5-level process in essence repeats this base sequence a minimum of 5 times. Details of the Sandia baseline 4-level polysilicon surface micromachining technology are described by Schriner [3]. The major impediments to advancing a multi-layer surface-micromachining process were surface topography and film mechanical stress.

Vertical Topography

Vertical topography is introduced by the repetitive deposition and etching of multiple films. The etch process creates film steps which normally are retained through the remainder of the process. This topography can produce mechanical interference between moving parts, and complicates subsequent process steps. For example, mechanical interference arises when interconnecting links must pass over a structure's edge. Figure 1 illustrates how these steps cause mechanical interference. The subsequent film used to create an interconnecting link deposits conformally over these steps producing an overhang feature. This artifact can protrude far enough into the lower levels to create mechanical interference. Without planarization of the surfaces, link/gear interference must be accommodated by design.

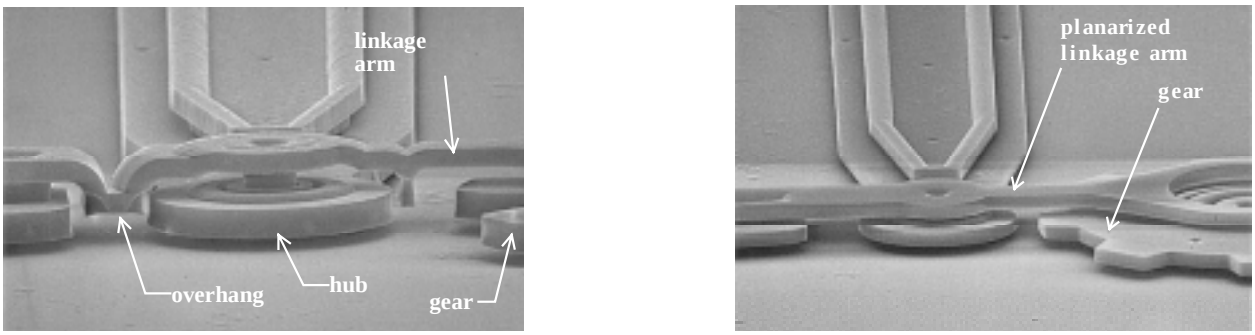

Figure 1. This SEM illustrates the artifacts generated by the conformal nature of the polysilicon depositions over prior topography (indicated by arrows).

In addition to the above design constraint, two significant process difficulties arise from severe topography. One is the result of the use of highly anisotropic plasma etch processes for the definition of the polysilicon layers. The anisotropy is necessary to obtain the desired vertical sidewalls of the polysilicon structures. However, the etch anisotropy prevents complete removal of the polysilicon layer from along the bottom edge of a step. This leaves behind long slivers of polysilicon along these edges, often referred to as stringers. Stringers can also produce mechanical interference or even electrical shorts. The second difficulty is problematic definition of subsequent layers over severe topography. Photoresist, the photosensitive polymeric coating used to transfer the design into the physical films, becomes difficult to apply, expose, and develop, leading to loss of resolution and definition.

The addition of chemical-mechanical polishing (CMP) planarization to the 4- and 5-level technologies is a major process enhancement from both the design and process perspectives [6]. The benefits of CMP for surface-micromachining are three-fold: it eliminates the link/gear interference problem illustrated in Figure 1, and it eliminates the artifact of anisotropic etching of conformal polysilicon films over edges, i.e., stringers, since there are no steps on a planar surface. Thirdly and most critically, CMP enables evolution to a multi-level technology such as the 5-level process by eliminating the topography and associated photolithographic problems.

Mechanical Stress

The second critical area involves control of the overall mechanical stresses present in the wafer due to the multiple film stack. The primary concerns being wafer breakage and excess wafer deformation. Although breakage is clearly catastrophic, excess wafer deformation in the form of bow or warp precludes continued processing of the wafer due primarily to wafer handling problems in the tool set.

Reduction or compensation of the film stresses on the wafer must not compromise a desirable stress state of the released mechanical parts. Specifically, two stress states must be controlled: first, residual net in-plane stress of the film is usually desired to be very low and tensile, which eliminates the possibility of mechanical buckling in structures, and second, a gradient in stress through the thickness of the film will cause excessive curl. In this new 5-level technology, the 5th layer continues to display the same degree of extremely low film in-plane stress and stress-gradient. The net in-plane stress is at the limit of the current stress diagnostic structures, which detect film stress at the tens of megaPascal level [7]. This implies that structures having extremely large in-plane dimensions continue to be viable in the 5th level of polysilicon. The polysilicon film processes exhibits a film curl having less than 150-nanometer out-of-plane deflection at the tip of a singly-clamped cantilever beam with a length of 1000 microns. This measurement is done using an interferometric technique [8]. Film distortion at this extremely low level is very acceptable even in optical mirror applications.

4. The Resulting Process

Referring to Figure 2, the cross-section of a device designed for the 5-level process clearly depicts all levels and illustrates planarization by CMP prior to polysilicon levels 4 and 5. Total stack height from the substrate dielectric layers is over 12.5 μm. The greatest device thickness that can be produced is 12.0 μm. In contrast, single level processes normally consist of polysilicon film thickness on the order of 2 μm. Thus, the stack is roughly a factor of 6 thicker which, from simple elastic beam theory, implies roughly a cubic increase in out-of-plane stiffness, i.e., greater than a factor of 100 increase in out-of-plane stiffness.

6. Summary

In summary, a 5-level polysilicon surface-micromachining technology that has extremely desirable mechanical attributes and expands the available mechanical design space has been developed. Initial results show that the addition of the 5th level of polysilicon provides both significant improvements in device reliability and robustness, and opens an entirely new design space.

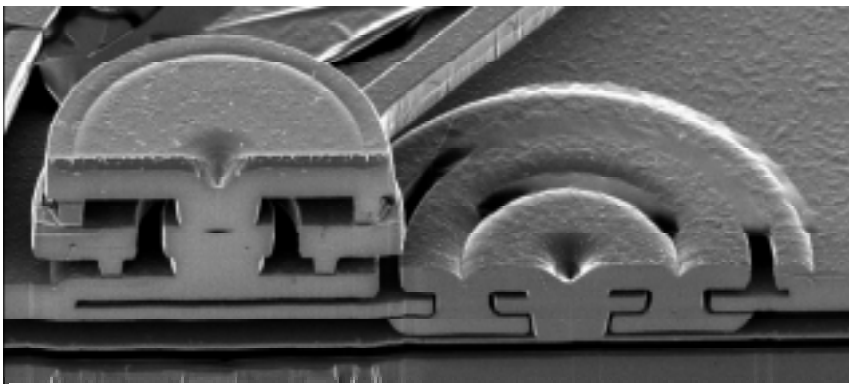

Figure 2. A scanning electron micrograph of a set of linkages to a rotating gear produced by focussed ion beam milling. The light contrast films are the polysilicon layers while the dark regions are the gaps in the free-standing structures.

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